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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,523	02/02/2001	Chun Chen	M4065.0390/P390	6271

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EXAMINER
BEREZNY, NEAL

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,523	CHEN, CHUN	
	Examiner	Art Unit	
	Neal Berezny	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-14,16-22 and 24-50* is/are pending in the application.

4a) Of the above claim(s) *25-50* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-14,16-22 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *02 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 9-14, 16-22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (5,482,881) in combination with Gardner et al. (6,127,235). Chen teaches a method of forming a source region in a substrate, fig.3, el.300, fig.1, el.132 and 116, comprising forming a pair of gate structures which extend in a first direction over a substrate, el.700, altering the upper surface profile of said substrate to form alternating areas of higher substrate surface elevation and areas of lower substrate surface elevation along said first direction and between said pair of gate structures, fig.3, el.300, providing a first doped layer in said substrate between said gate structures, which has a profile which follows that of said upper surface profile and providing a second doped layer in said substrate between said gate structure, which is below said first doped layer and which has a profile which follows that of said first doped layer, fig.4d, el.130, wherein at least one of said areas of higher and lower substrate surface elevation is doped by said first doped layer to act as a source region of a transistor, fig.3, el.300, wherein said area of higher substrate surface elevation acts as a source region, fig.3, el.300, wherein said second doped layer is provided in said substrate before said first doped layer, col.6, ln.55-63. Chen also teaches a method of

forming a plurality of dopant pockets on a substrate, fig.1, el.130, 116, comprising forming a plurality of implantable regions on said substrate separated by field oxide regions, Fig.3, el.300, said implantable regions and field oxide regions extending in a first direction, forming a plurality of word lines located over said implantable regions and field oxide regions, el.700, said word lines extending in a second direction perpendicular to said first direction, selectively etching, col.6, ln.55-60, and removing portions of said field oxide regions between two adjacent word lines to expose respective substrate regions, el.302, col.6, ln.16-22, forming source regions in said implantable regions, fig.4d, el.132, co.7, ln.1-5, implanting a dopant into said substrate through said respective substrate regions to form said dopant pockets beneath said source regions, el. 130, col.6, ln.55-63, wherein said dopant is a n-type dopant, col.6, ln.55-60, wherein each of said word lines is formed of a gate stack comprising a gate oxide, a floating gate, a dielectric formed over said floating gate, and a control gate formed over said dielectric, el.120, 122, 124, and 126, wherein said act of implanting said dopant is carried out with an implanting energy higher than implanting energy used to form said source regions, col.6, ln.55-63, said act of implanting said dopant employs directing said dopant through said substrate region at an angle of substantially 90 degrees incidence to said substrate region, fig.6c, el.MDD1, wherein said act of implanting said dopant employs directing said dopant through said substrate region at angles different than substantially 90 degrees incidence to said substrate region, fig,8d, el.MMD1, wherein said act of implanting boron into said substrate is carried out after said act of removing said field oxide material, fig.3, el.302,130.

3. Chen does not appear to specifically state that said act of implanting said dopant into said substrate is carried out after said act of forming said source regions, nor the use of a p-type dopant, such as Boron, nor employing a BF_2 dopant source, nor the use of a photoresist mask for both the source region and the dopant pocket implants. Chen does teach the use of a generic "first conductivity type", col.11, claim 4, thereby suggesting to one skilled in the art that Chen anticipated the use of both N-type and P-type dopants.

4. Gardner et al. (6,127,235) teaches the source implant first and then the pocket implant second, fig.1d and 1f, el.122 and 152, respectively, col.4, ln.61-66, and col.5, ln.20-27. Further, Gardner teaches the interchangeability of P-channel and N-channel device processes, clearly identifying the use of boron dopant, coi.8, ln.13-16. It is well known in the art to use different dopant types to build both NMOS and PMOS devices by using both types of dopants, in order to build CMOS devices having lower power consumption. Further, it is well known in the art that Boron is commonly used as a P-type dopant and that BF_2 is a well-known dopant source. It would be obvious to one of ordinary skill in the art at the time of the invention to use boron and BF_2 for a P-type dopant because of its compatibility with silicon crystal structure as a doped semiconductor. Finally, it would be obvious to one of ordinary skill in the art at the time of the invention to combine Gardner with Chen so as to modify Chen's order of implants from deep and then shallow to shallow and then deep. Both methods, as suggested in the prior art of Chen, fig.1, el.130, 132, and 114, and further elaborated in Gardner, are well known in the art to be equivalent processes. Recall that Chen improves the

process of the prior art of Chen by changing the order of the implants in order to eliminate an expensive masking step. The prior art of Chen recognizes that the order of implants has little impact on the overall process results or process costs and efficiencies, when using the conventional process of Chen's prior art and when building a single device type, ie. a peripheral transistor only. A skilled artisan, using the teachings of Gardner and Chen would be motivated to employ either sequence of implants in order to provide greater process latitude when building and designing a process for peripheral devices that are built coincident to other device structures that may require a shallow implant first so that a masking or etching step could be performed prior to the deep implant, thereby allowing the same implant to be performed on both devices reducing process steps and costs.

5. Although, Chen does not teach using the same resist mask for both the source region and dopant pocket implants, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the prior art of Chen with the Chen invention to anticipate applicant's claimed invention. Recall that Chen's invention improves the prior art process of Chen by building a memory transistor and the peripheral transistor from two separate processes to a single more efficient process. The reason that Chen removes the resist after the DDI implant and before the MDD implant is to that the peripheral devices could also be built without additional masking and processing steps. It would be obvious to an ordinary artisan, using the teachings of Chen and Gardner, to build a single device type by using the same resist mask for both implant steps, so as to reduce damage to the oxide layers caused by implanted ions creating the "knock on"

phenomena resulting in increased leakage currents into the substrate, thus requiring more frequent refresh times and increased power consumption.

Response to Arguments

6. Applicant's arguments with respect to claims 1-7, 9-14, 16-22, and 24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Neal Berezny whose telephone number is (703) 305-1481. The examiner can normally be reached on M-F 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NB
June 25, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800